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PATENT SPECIFICATION

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(54) IMPROVEMENTS IN AND RELATING TO ELECTRONIC NUMBER SELECTORS

(71) I, CHARLES FRANCIS McCRORY, of 4, Silksworth Row, Sunderland, Co. Durham, a British Subject, do hereby declare the invention, for which I pray that a patent may be granted to me, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to improvements in and relating to random number selectors.

Random number selection is often used in games of chance such as prize draws, to select the winner of a prize, or other reward. Manual selection is feasible, and much practised, by placing for example numbered counterfoils of numbered tickets in a drum, rotating the drum a few times to thoroughly mix the counterfoils, and manually withdrawing one or more counterfoils from the drum. It can be argued that this method is not truly fair, since counterfoils to one side or other of the drum may have less chance of being selected than those directly beneath the entrance.

Mechanical number selectors are also known for example wherein drums displaying numerals or other devices are rotated, and randomly arrested so that a number is formed by the numerals displayed at a series of windows, and is declared the winning number.

A disadvantage of such mechanical devices is apart from the possibility of breakdown, that it is difficult or impossible to arrange for selection among a series of number having a minimum higher than nought, and a maximum lower than e.g. 999 for a three drum machine. However, as draw tickets at for example a club, may be sold from the same series of numbers on successive nights, with previous sales, and unsold tickets to be excluded, it is essential to be able to prevent the device from selecting an excluded number, and to be able to flexibly program the device for various maxima and minima from one occasion to the next.

The invention provides an electronic number selector, comprising a pulse generating circuit for generating a train of pulses, a counter for counting said pulses, the counter comprising one or more counter stages, each having a corresponding numeral indicator for displaying the count attained by the respective counter stage, an adjustable minimum switch for each stage for predetermining the starting value of a counting sequence, and an adjustable maximum switch for each stage for predetermined the upper limit of the counting sequence, the maximum switches being interacting so that they act to stop the counting sequence when all the counter stages reach their maximum counts together, and start a further counting sequence from the preset minimum, means for starting the counting, and/or the production of pulses, and means for stopping the counting and/or production of pulses at an arbitrary moment, the counting proceeding from minimum to maximum repeatedly and continuously between the operation of the starting means of the stopping means.

Any number, for example five, counting circuit stages with corresponding numerical indicators can be employed.

A minimum switch and a maximum switch is preferably provided for each counting stage, in order to preset the minimum and maximum numbers, and define the numerical limits of the count.

A gate circuit may be provided for resetting the stages to their preset minima, connected to each of the maximum switches, so that when all the maxima are reached together, indicating attainment of the maximum count, the gate is triggered.

The clock circuit may be modified to provide irregularly or regularly space long pulses, so that the count is held up for a tenth of a second, or so, that the display can be perceived to change, the normal pulse frequency being preferably above 5kH$_z$.

The invention will now be further described by way of example, with

reference to the accompanying drawings, wherein:

Fig. 1 is a block circuit diagram of a preferred embodiment of the invention;

Fig. 2a is a wiring diagram of a modified form of pulse generating circuit;

Fig. 2b illustrated diagrammatically the form of pulses generated by the circuit in Fig. 2a; and

Fig. 3 is a circuit diagram illustrating a remote control for initiation of the operation of the pulse generator.

As shown in Fig. 1, the random number selecting device according to the invention comprises a series of counter stages 10a to 10n, one for each decade to be counted, and of which only the first 10a and the last 10n, are shown, for clarity. The counters stages count the pulses emitted from a clock circuit 11, which includes a clock gate 12.

The counters stages 10a—10n feed information to binary to decimal converters 13a—13n, which each drive a respective solid state digital display 14a—14n. By means of multi position minimum switches 15a—15n, each driven by a thumbwheel, it is possible to set a number from which the count will start, i.e. a lower number. Similarly multi position maximum switches 16a—16n are set, also by thumbwheels, to a maximum figure above which the count cannot progress.

The power supply to the device comprises a 240 volts A.C. mains input connected to the primary 20 of a transformer. The transformer has a high tension secondary 21. connected between earth and the display devices 14a—14n, to power the displays. This winding 21 develops a voltage of 180 volts, and is connected to a diode 22 which suppress the negative component of the A.C. current, producing a pulsed d.c. current of corresponding frequency.

The transformer also has a low tension secondary 23, which develops a voltage of 5 volts. The winding 23 is connected to a fullwave rectifier bridge 24, which produces a smooth d.c. voltage. This power supply is connected to the clock circuit 11.

A start switch 25 is connected between the input and earth, and the line from the input and switch 25 is connected to the base of a buffer transistor 26, the emitter of which is earthed.

In operation, the minimum switches 15a—15n are set to the desired minimum member, and the maximum switches are set to the desired maximum number. The clock circuit is initiated by the switch 25, and the pulses generated are fed by a line 27 to each of the counters 10a—10n. The counter stage 10a counts each pulse, while the second counter stage (10b, not shown) counts each tenth pulse, and so on, while the counter stage 10n counts each $10^{(n-1)}$th pulse. The count in counter stage 10a starts from the preset minimum (e.g. 3) until the end of the first shortened, decade is reached, but each succeeding decade is counted in full from θ to 9. The higher order counters operate similarly. When the preset maximum in each decade is reached, a pulse is fed through the appropriate contacts of maximum switch 16a—n to one input of an AND gate 30, which has a separate input from each maximum switch. The AND gate 30 is only opened if all the inputs are high simultaneously, otherwise the count proceeds in the counter 10a—n normally. This is important, as the maximum in the first decade will be reached with every 10th pulse, in the second with every hundredth, and so, while the maximum in the final decade will only be reached once in each counting sequence. This prevents any premature restarting of the count, and ensures that all relevant numbers will be included.

When the gate 30 is enabled, a pulse is applied to a reset line 31, connected to each minimum switch 15a—15n, and counter 10a—10n which resets the counter to the minimum, and restarts the count from the minimum. These sequences can be repeated several times before the selection is made.

After an arbitrary period, it is necessary to stop the count in order to select one number from the sequence. This is done by applying a potential to an input 32 which blocks the operation of the clock circuit 11, When the clock circuit 11 ceases to produce pulses, the count halts, and the digits displayed by units 14a—14n are "frozen". The number so displayed is treated as the number selected.

The potential used to halt the count, may be controlled by a switch which, in order to produce a random element, is controlled by an inexact timing device, for example a latch device with an unpredictable decay time, such as a suction holding device with an air leak.

After the selection operation, the counter may be reset to zero by operation of a zero switch 33, and then the minimum switches used to set a new minimum to prepare for a further selection operation.

In Fig. 2a is shown the circuit of a modified clock 11, wherein a clock gate 40 is connected to 5 volts d.c. input 41, has two other inputs 42 and 43, each connected between a common earth, and an output 44. The circuit of input 42 includes a resistor 45, and a capacitor 46, and the circuit of input 43 includes a resistor 47, a diode 48, and a capacitor 49. The lines to the inputs 42, 43 pick up pulses from the output, and use these to modulate the pulses

produced by the gate 40. The resulting pulse form is shown diagrammatically in Fig. 2b wherein the normal duration pulses 50 (kH_3) are interrupted irregularly, or regularly, by longer pulses 51, which endure for several beats of the normal frequency. The purpose of this is to periodically halt the count to freeze the display on display units, 14a—14n, so that the count can be seen to change. At the normal count rate, the tens and units at least would be invisible due to their rapid changes.

Finally, in Fig. 3 is shown a means whereby the device may be remotely actuated. A portable device 60 has a battery 61, a push button switch 62, and oscillator circuit 63, tuned to an ultrasonic frequency, and a condenser microphone 64. This microphone will, when the circuit 63 is actuated by switch 62, produce an ultrasonic sound beam, which can be picked up by a receiver 65, comprising an earthed condenser microphone, connected via an amplifier 66, a diode 67, and the base of buffer transistor 68. The collector of transistor 68 is connected to a 5 volts d.c. input, while the emitter is connected to the counting circuit 10.

When microphone 65 produces a current in response to the ultrasonic beam, this is amplified and applied to the base of transistor 68 which becomes conductive and allows the power input to pass to the clock circuit 10. A latitude of modification of the device is of course possible within the scope of the appended claims. For example, the counter stages may be cascaded decade counters, which each count ten input pulses, and then emit an output pulse to a next succeeding counter. In the preferred embodiment, the counter stages are synchronous programmable counters.

It is of course possible to make several selections from the same sequence of numbers, as for example drawing for first, second and third prizes.

WHAT WE CLAIM IS:—

1. An electronic number selector, comprising a pulse generating circuit for generating a train of pulses, a counter for counting said pulses, the counter comprising one or more counter stafes, each having a corresponding numeral indicator for displaying the count attained by the respective counter stage, an adjustable minimum switch for each stage for predetermining the starting value of a counting sequence, an adjustable maximum switch for each stage for predetermining the upper limit of the counting sequence, the maximum switches being interacting so that they act to stop the counting sequence when all the counter stages reach their maximum counts together, and start a further counting sequence from the preset minimum, means for starting the counting, and/or the production of pulses, and means for stopping the counting and/or production of pulses at an arbitrary moment, the counting proceeding from minimum to maximum repeatedly and continuously between the operation of the starting means and of the stopping means.

2. A selector according to Claim 1, wherein each counter stage sends a pulse to gate circuit when the preset maximum for that counter stage is reached, the gate being enabled when all the counter stages send a pulse simultaneously, to effect restarting of the count at the preset minimum.

3. A selector according to any preceding claim which is remotely controllable by a manually operated device, having an ultrasonic transmitter which activates an ultrasonic receiver electrically connected to operate a switching transistor in the power supply circuit of the clock circuit.

4. An electronic random number selector substantially as hereinbefore described, with reference to and as illustrated in Fig. 1 of the accompanying drawings, or modified as illustrated in Figs. 2 and/or 3 of the accompanying drawings.

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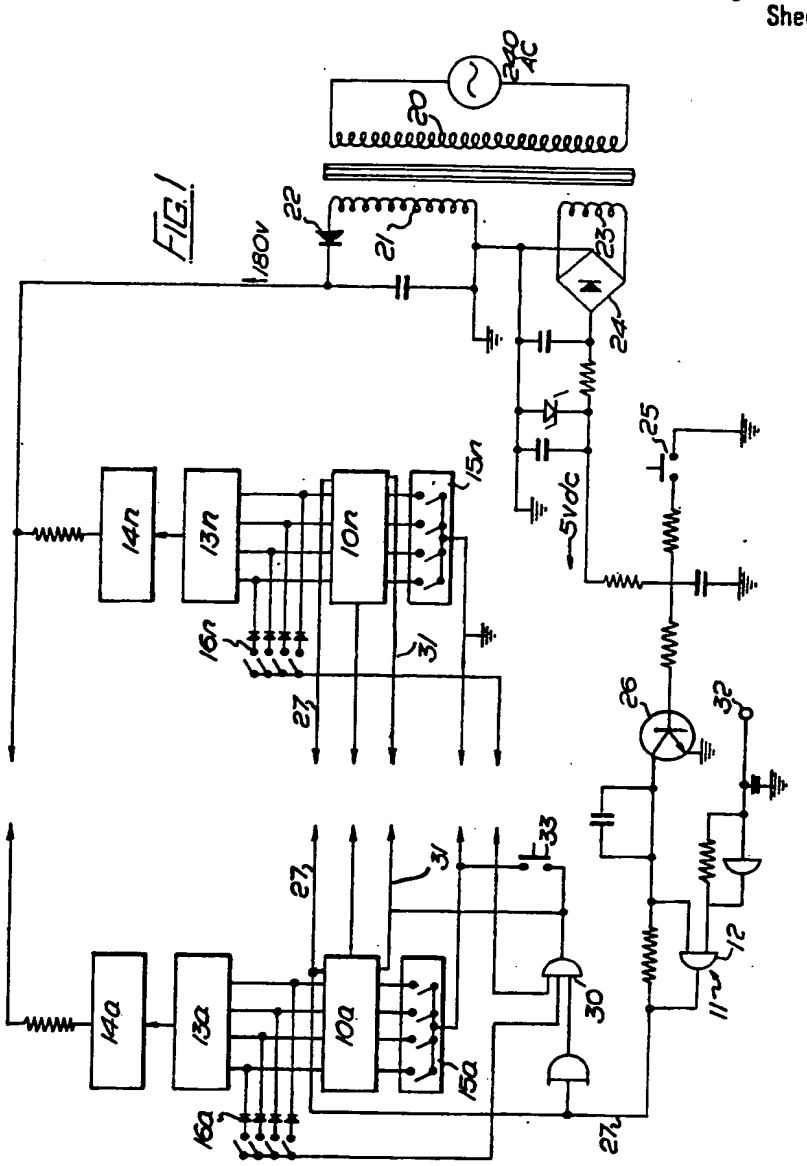
2 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheet 1

FIG. 1



1515282 COMPLETE SPECIFICATION
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Sheet 2

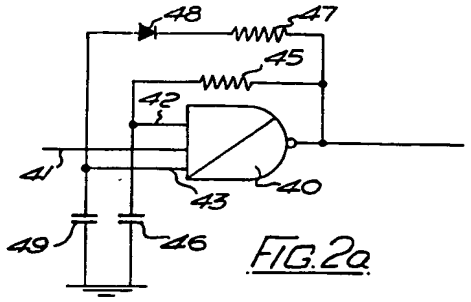

FIG.2a

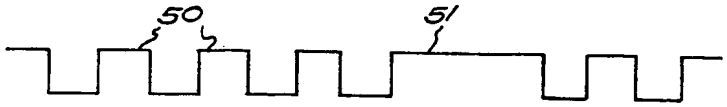

FIG.2b

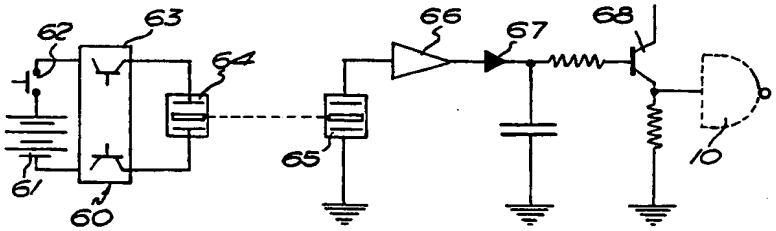

FIG.3